

Fig. 1
PRIOR ART

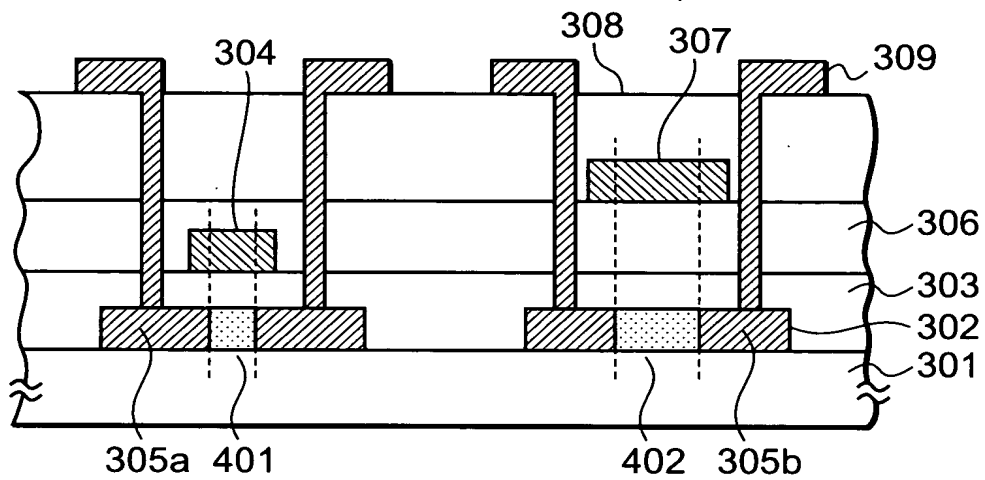


Fig. 2(a)

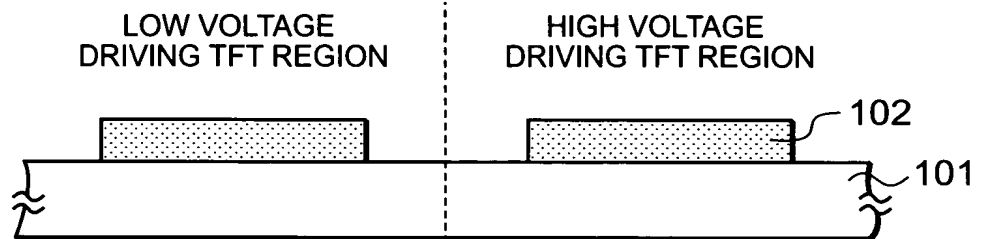


Fig. 2(b)

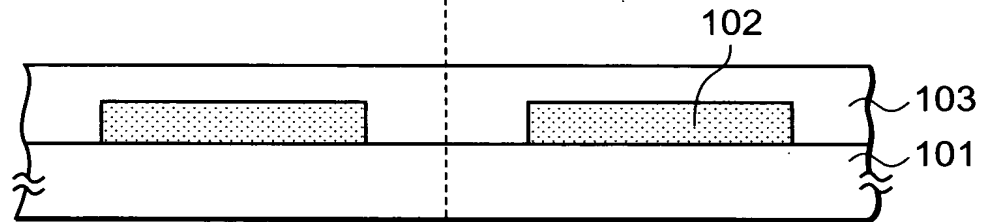


Fig. 2(c)

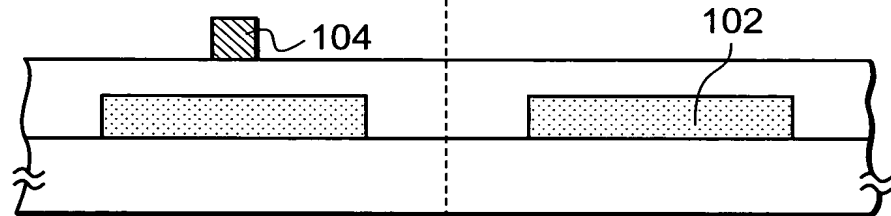


Fig. 2(d)

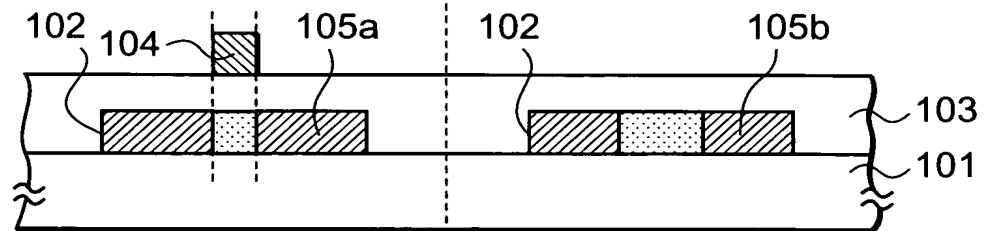


Fig. 3(a)

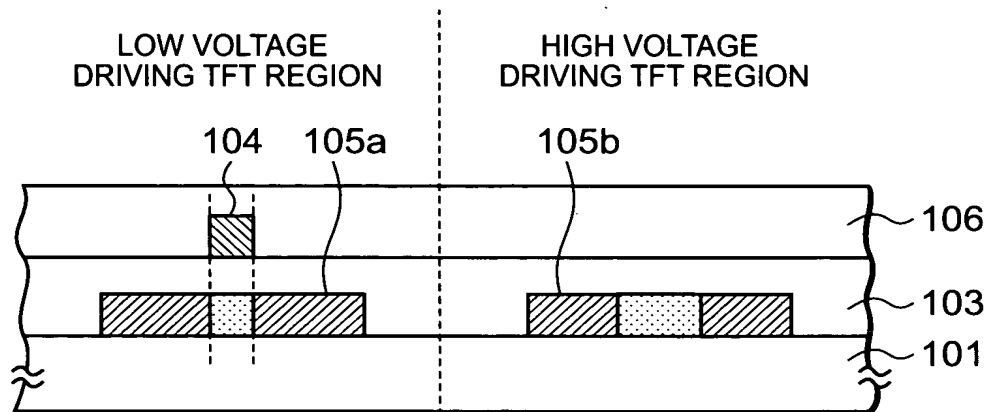


Fig. 3(b)

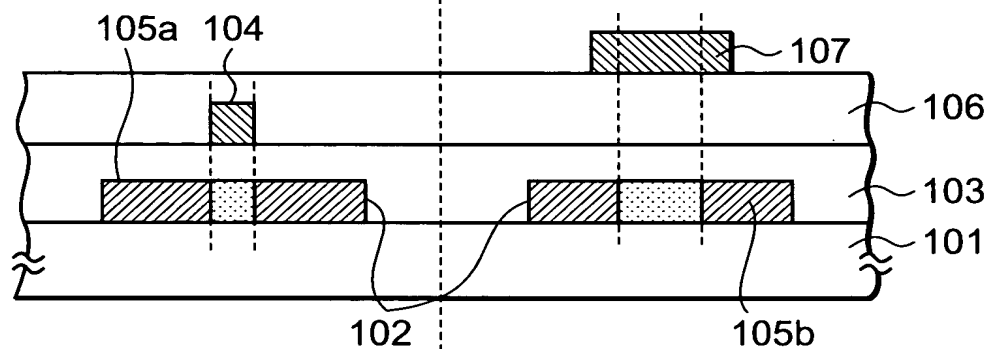


Fig. 3(c)

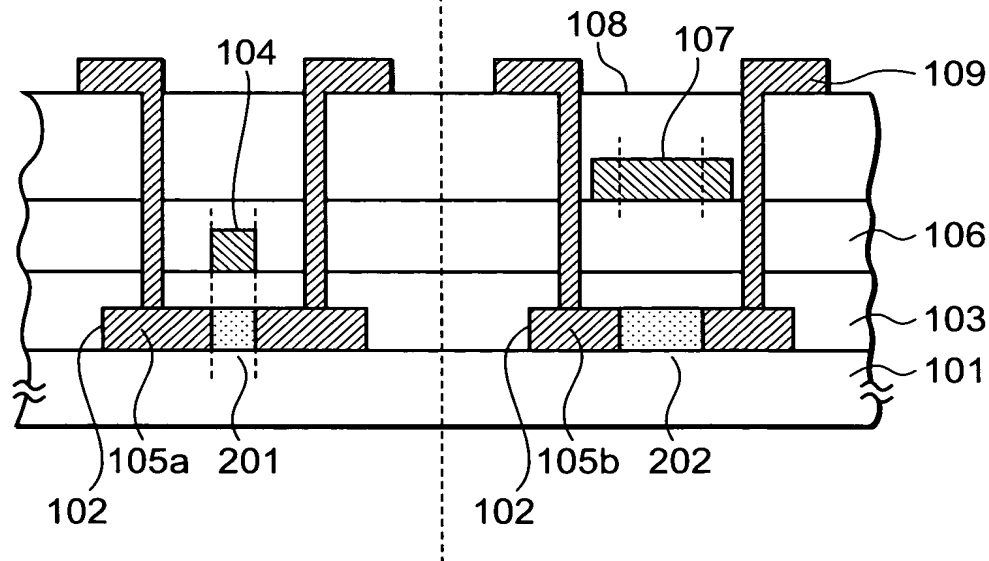


Fig. 4(a)

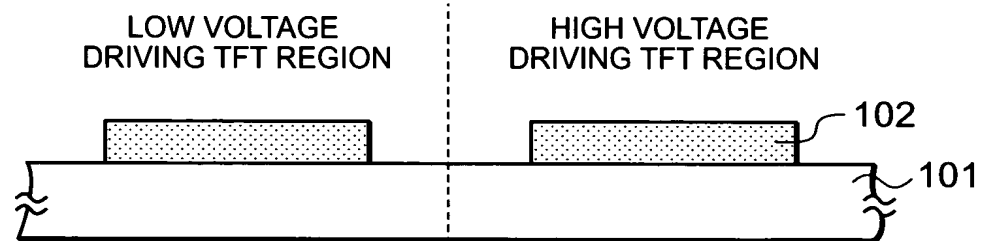


Fig. 4(b)

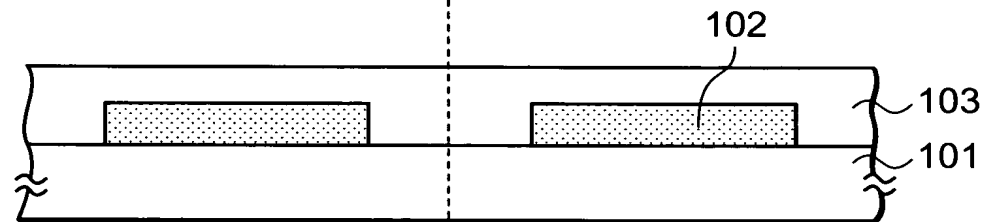


Fig. 4(c)

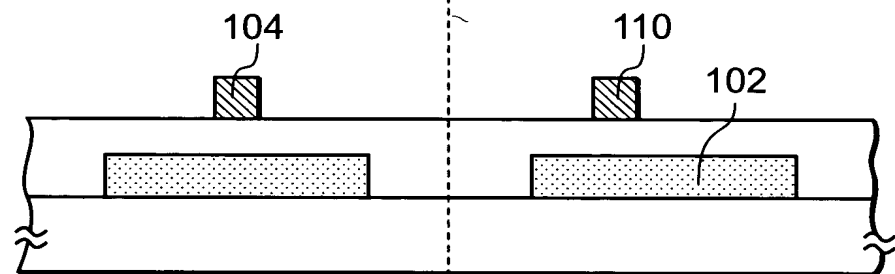


Fig. 4(d)

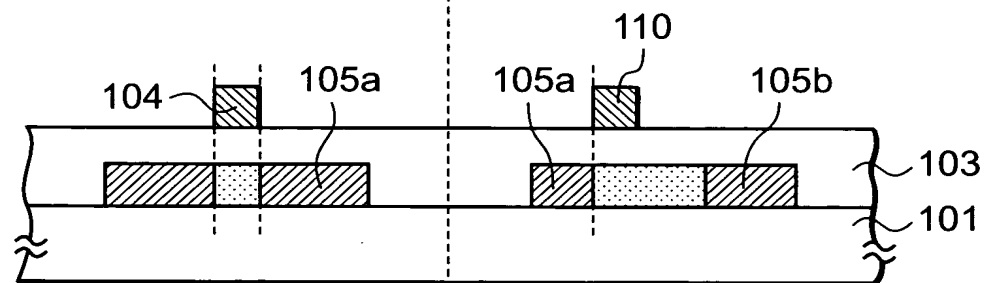


Fig. 5(a)

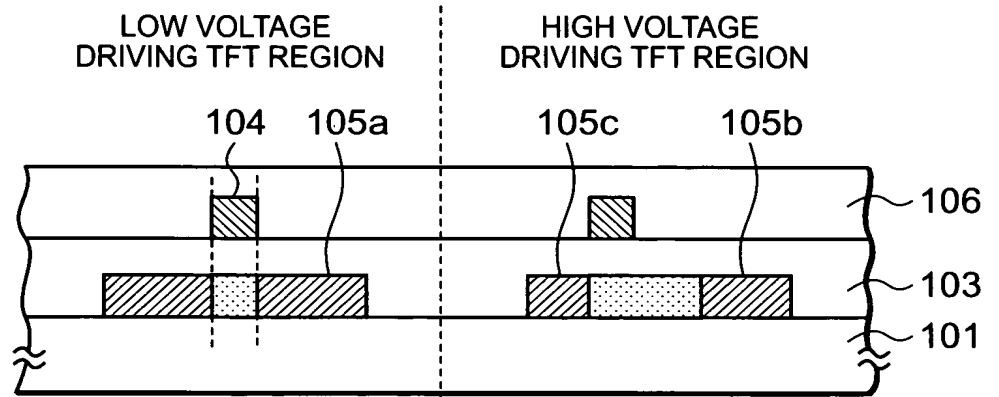


Fig. 5(b)

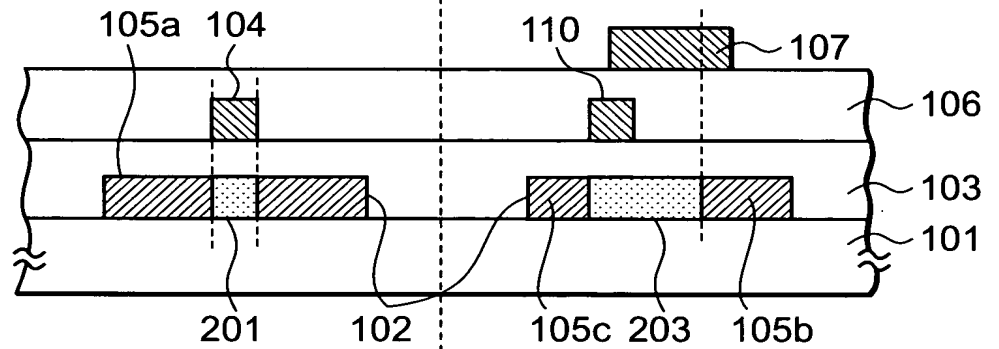


Fig. 5(c)

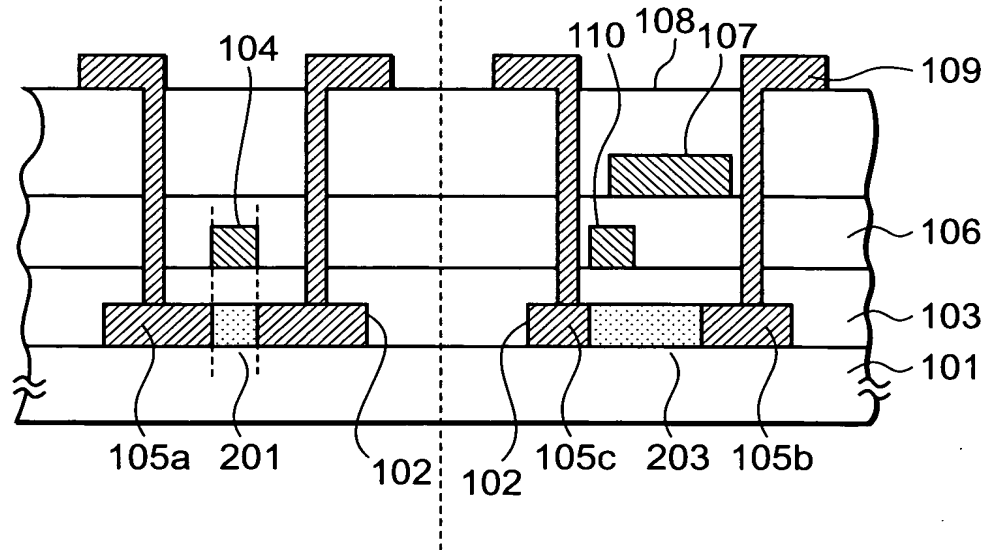


Fig. 6

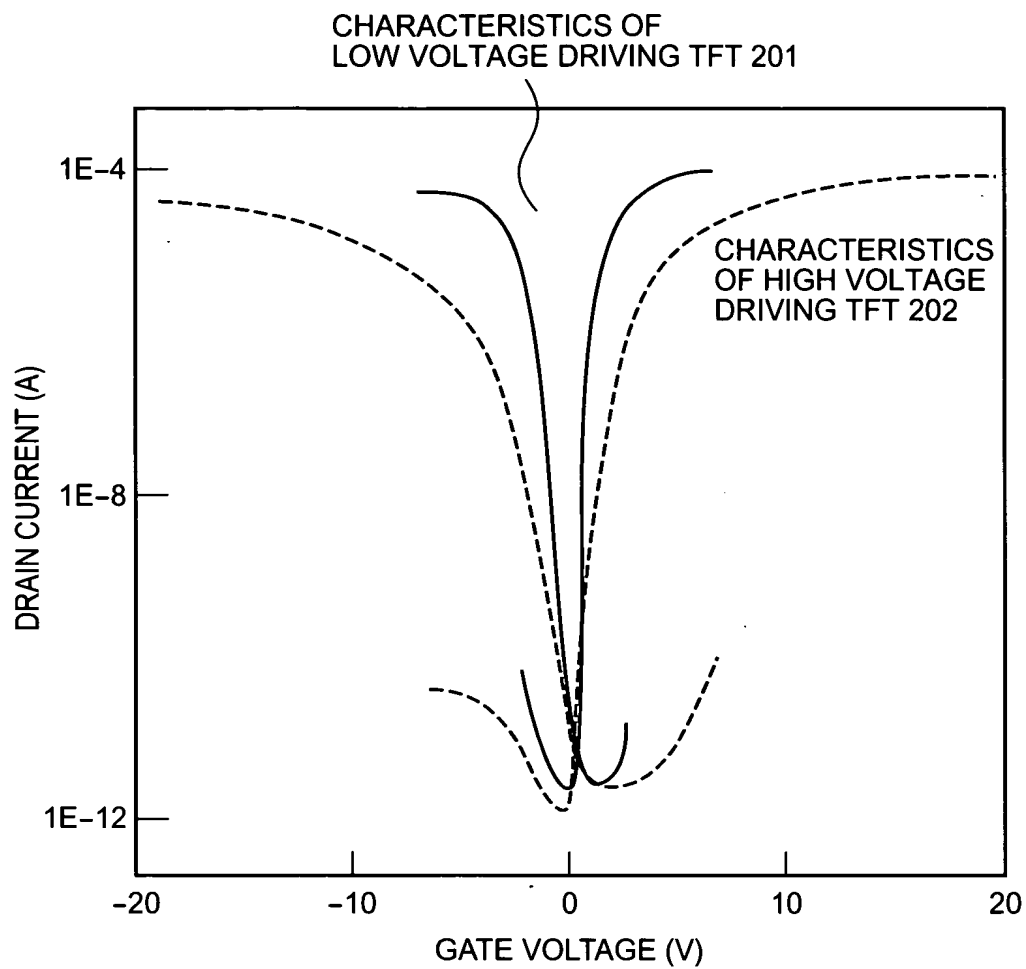


Fig. 7

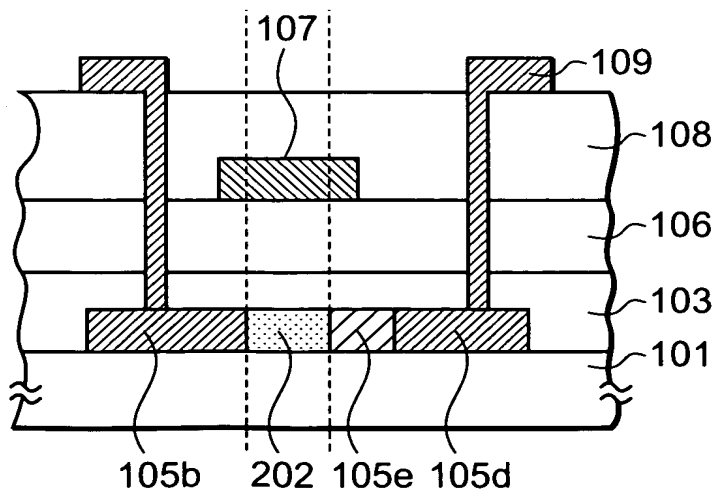


Fig. 10 is a cross-sectional view of a semiconductor device. It shows a central channel region 107 flanked by gate regions 108 and 109. The device is built on a substrate 101 with a base layer 103 and a top layer 106. A central region 203 is shown with a different pattern. Labels 110, 107, 108, 109, 106, 103, 101, 105c, 203, 105e, and 105d are present.

Fig. 10

